Project Final Report

CDA 4213 – F24

Section 005

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Final Design

Our final design consisted of 24 rows of 24 Carry Sum adders (full adder with AND gate). The design decision that allowed us to obtain this density was reorienting the AND gate (see below). From the initial planning stage, we knew we would be limited by available space on the X axis. So, if we can make each CSA squarer (increase height, decrease width), we could increase our density.

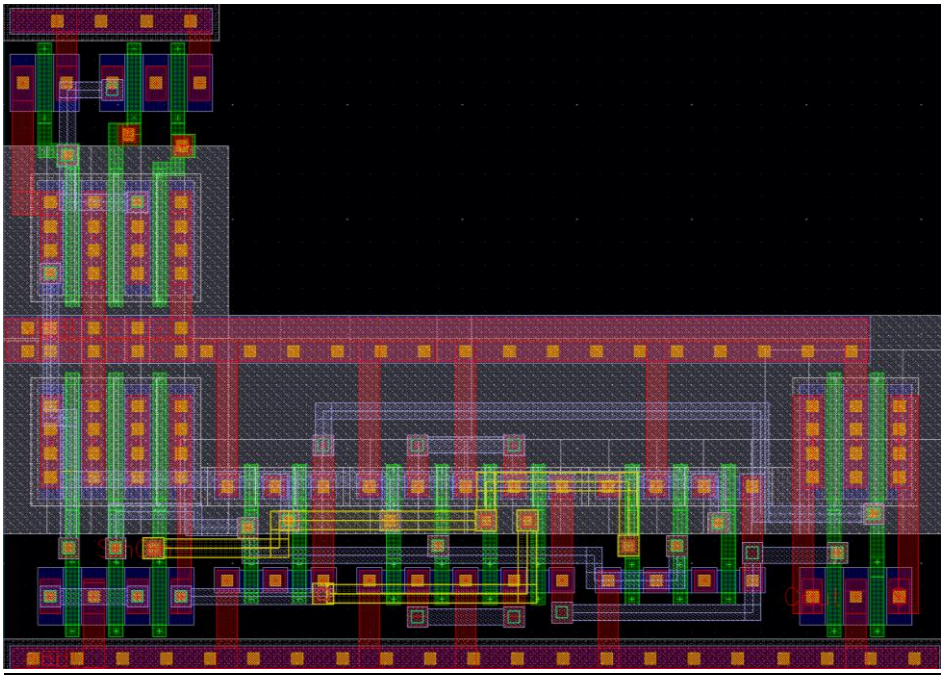


Figure 1: CSA Layout

To achieve the goal of minimizing component width, when combining CSA cells, we would flip cells processing even bits horizontally and vertically. However, this level of density meant that we would have a few additional challenges:

- Power Distribution
    - Due to the length of the row (620.5um), it would be likely that we'd have issues with power delivery to cells towards the middle of the layout. Due to now being more constrained by height, simply increasing the well size above and below each cell wasn't as appealing of an option. Thus, we created 'bus bars' down the middle of each row of CSAs, as well as down the left and right sides of the array.
- I/O Routing
    - Due to the interconnect complexity (8 inputs per 50um), we decided that pre-routing each row would be the most efficient way to reduce the workload of creating the final layout.

- Signal Strength
    - Because of the distance each bit would be expected to travel horizontally, and the draw on that input line, we made the decision to include signal boosters (dual invertors).

With those challenges, we arrived at the final layout pictured below.

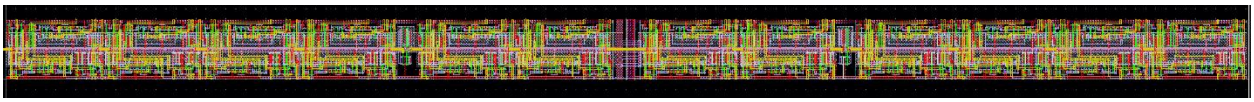


Figure 2: Final CSA Row Layout

Zooming in on the boosters and power bars,

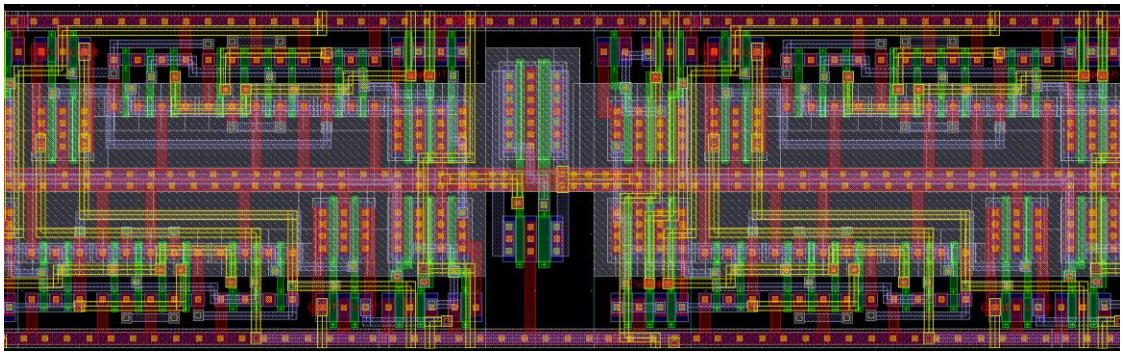


Figure 3: Zoomed in view of CSA with Y Booster

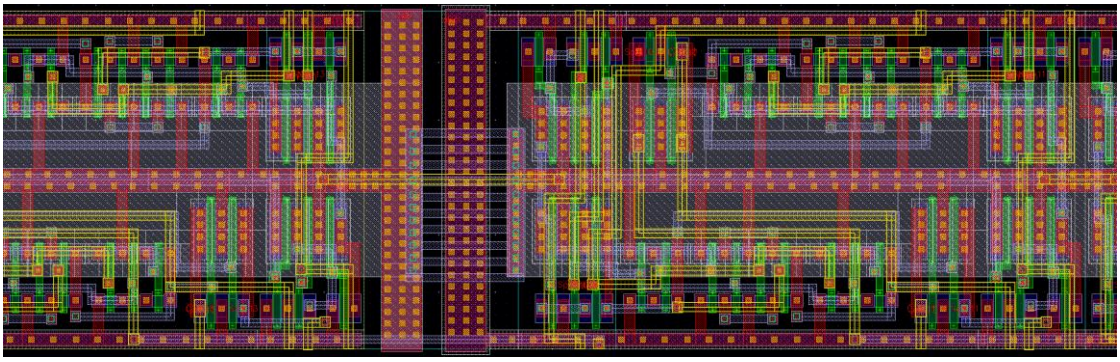


Figure 4: Zoomed in view of CSA with vertical power bars

Seeing similar possible problems with the inputs across the X axis (especially with the line complexity within each cell; the inputs are not necessarily taking the shortest possible path), we decided to create a 'booster row', to amplify the signals across the X axis. Including the CSA routing in this cell, as well, we arrived at the below layout.

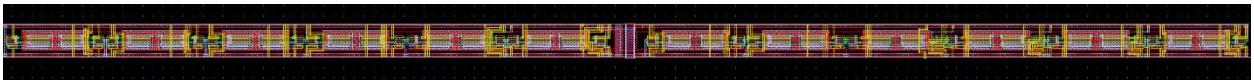


Figure 5: X booster row

Below, you can see a closer view.

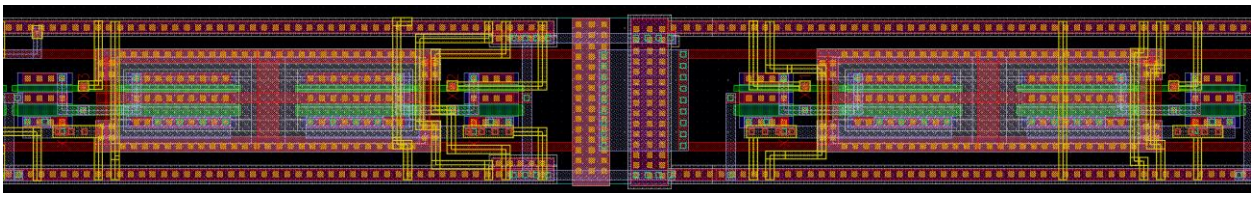


Figure 6: Zoomed in view of X Booster row, with power bars

For power distribution on the X booster row, the GND bars are top/bottom to interface directly with the CSA rows, and we have one VDD guardring around every 4 PMOS cells, with power input on the left and right sides as well as from the center bar.

The CPA row is simply a row of full adders. Below is the final layout for the CPA row.

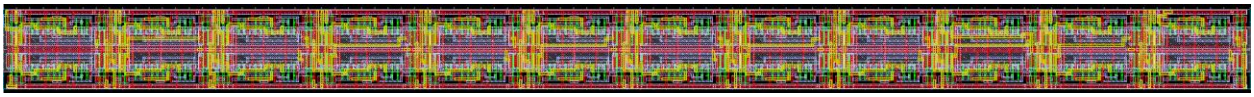


Figure 7: CPA Row layout

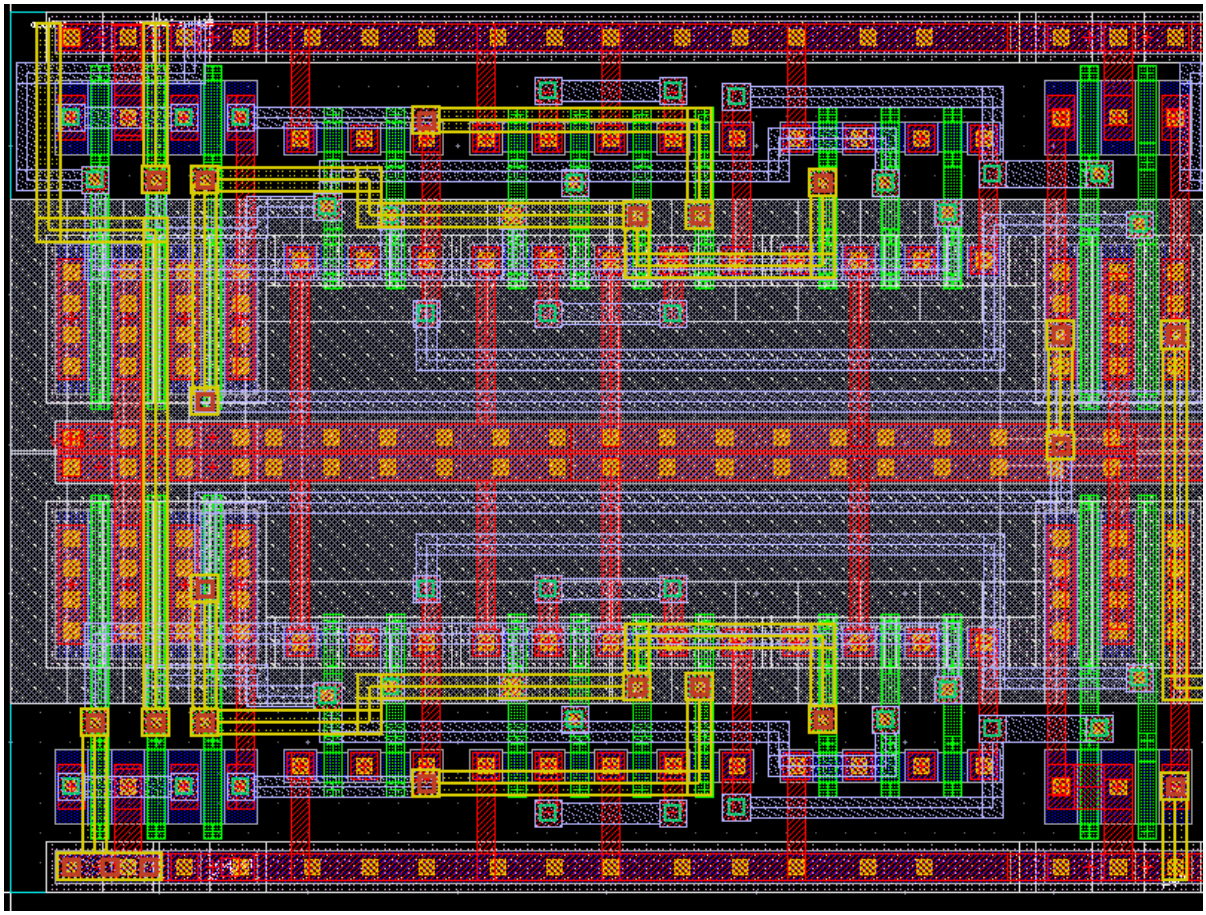


Figure 8: View of two combined CPA (full adder) cells in CPA row

For controlling the registers (figure 9) we elected to use one OR gate (NOR + Invertor) per register. This meant that theoretically, with only a CLK and EN signal, we could control I/O on each register. When EN is sent, the CLK input to each gate is held HIGH and CLK_NOT low, freezing the registers. Additionally, due to the design of our register, we could use the same registers for both the input and the output. Because of the same signal strength issue, we included two invertors in the middle of each register. One invertor would invert CLK to CLK_NOT with renewed strength, the other CLK_NOT to CLK. Only using one invertor per signal also means that the CLK signals should remain in time.

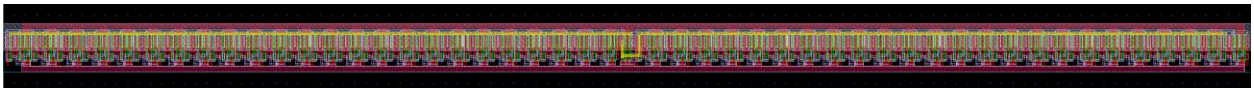


Figure 9: Register

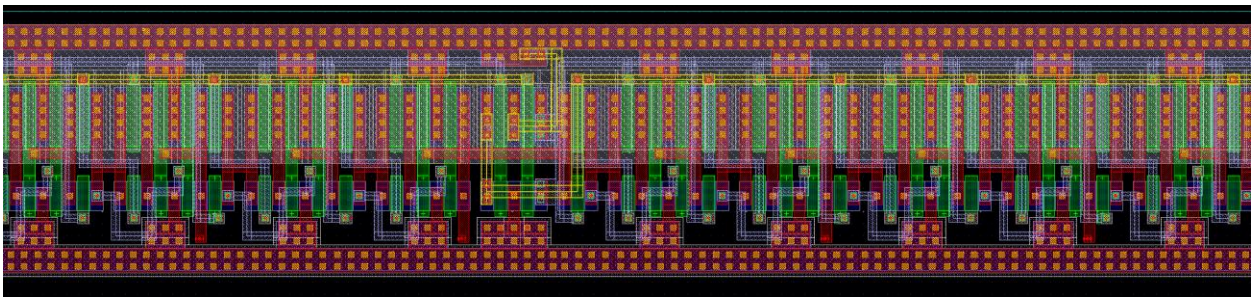


Figure 10: Register, picturing CLK invertors (middle)

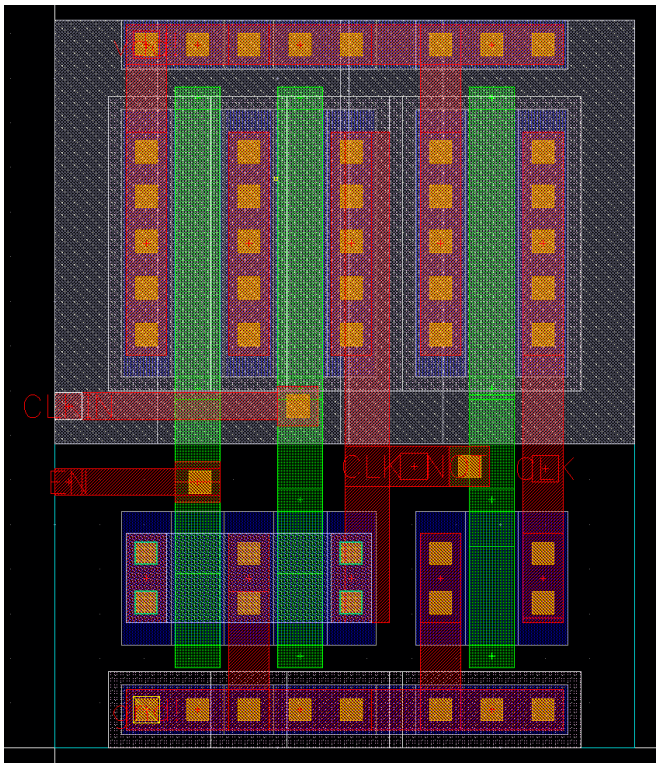
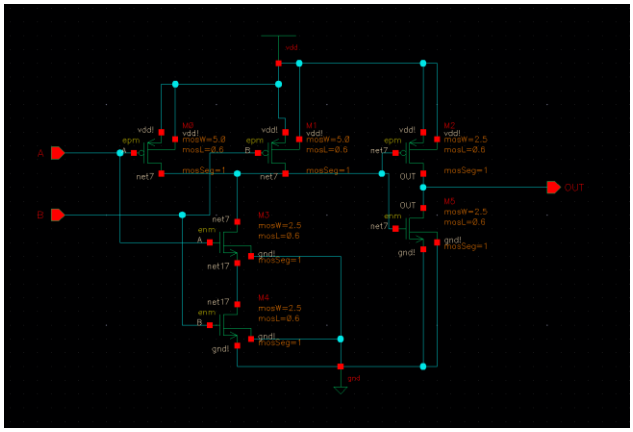


Figure 11: CLK Controller

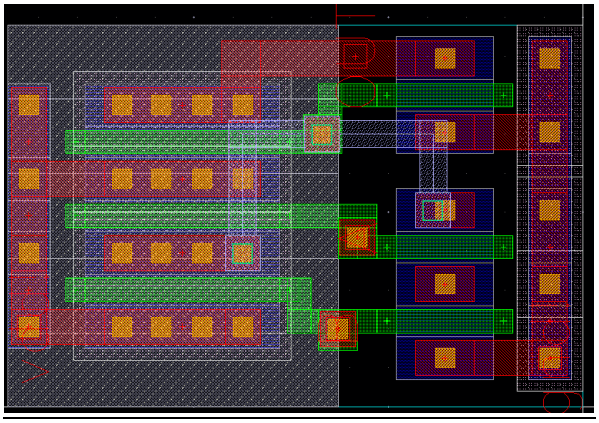
Final Cells

AND Gate

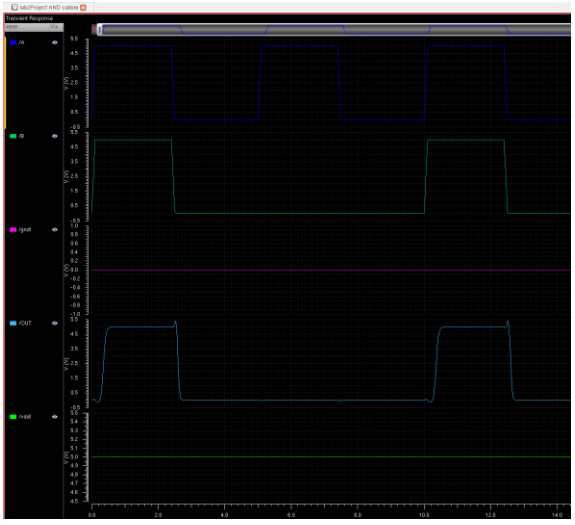
- Schematic



- Layout

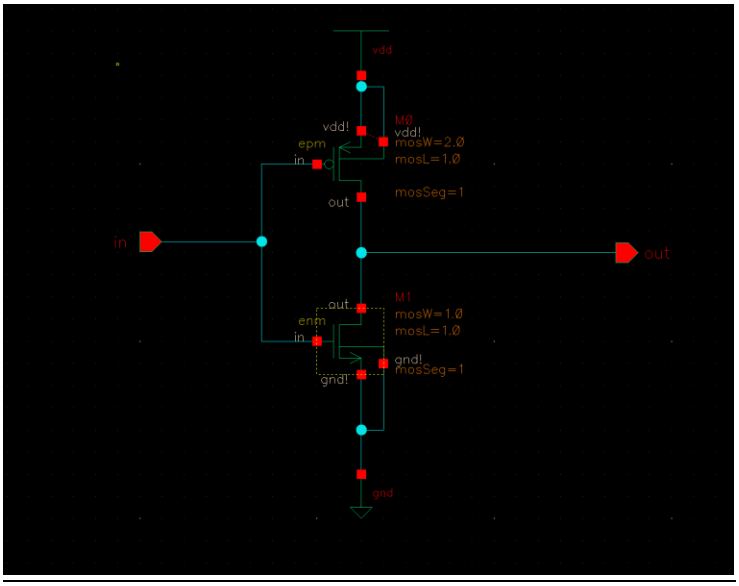


- Simulation

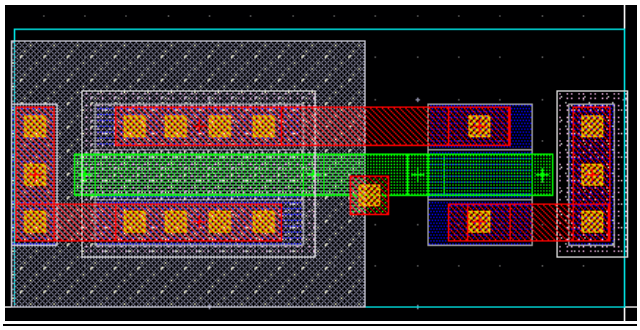


Invertor (Used in Boosters)

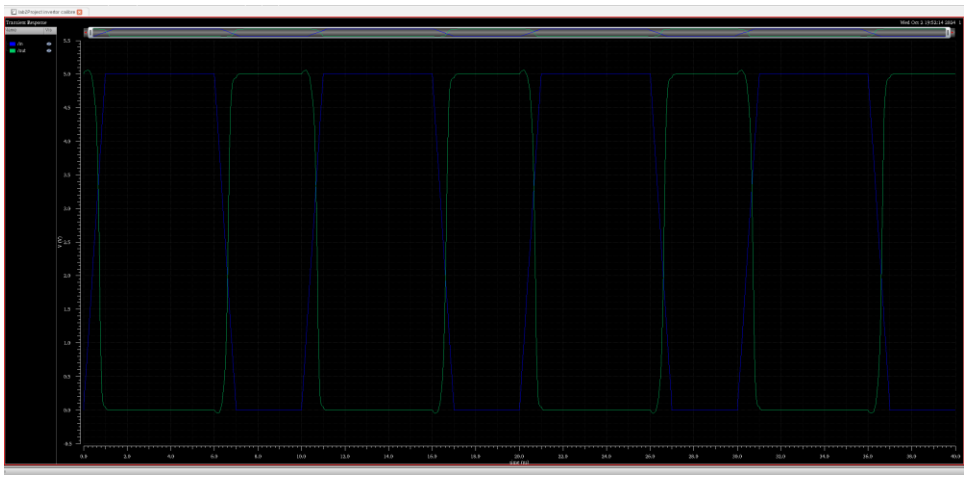
- Schematic



- Layout

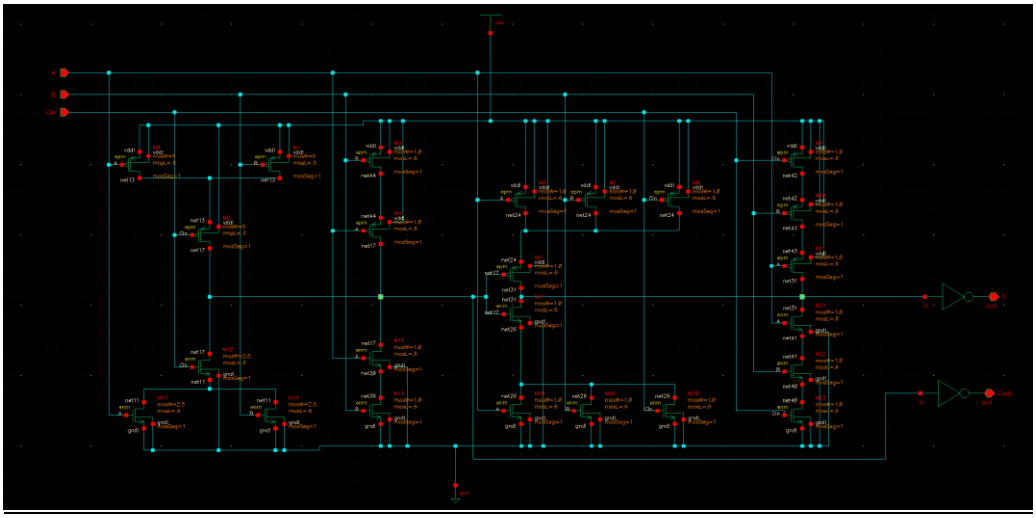


- Simulation

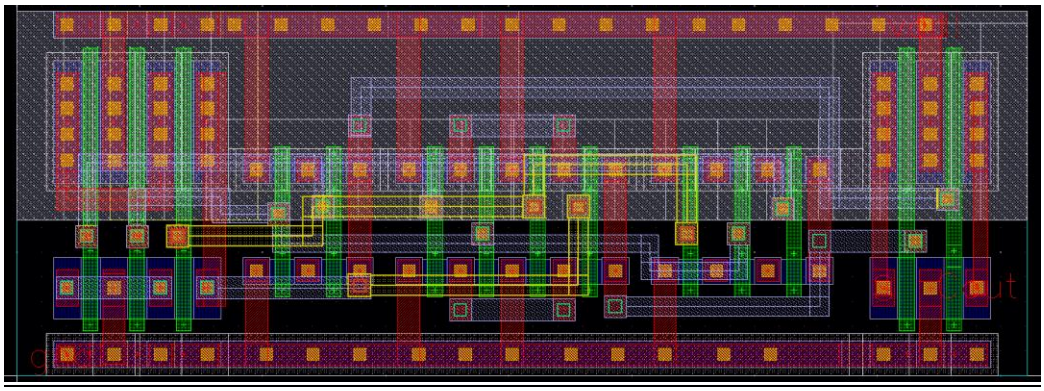


fullAdder

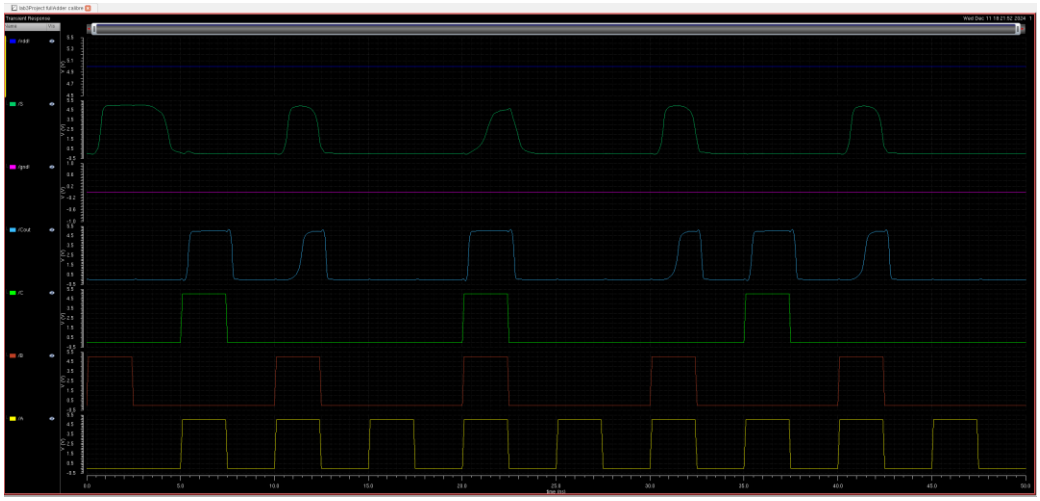
- Schematic



- Layout

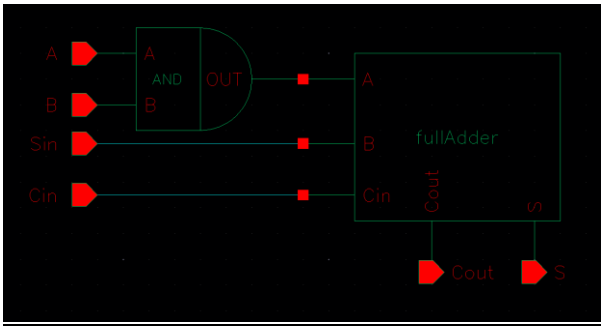


- Simulation

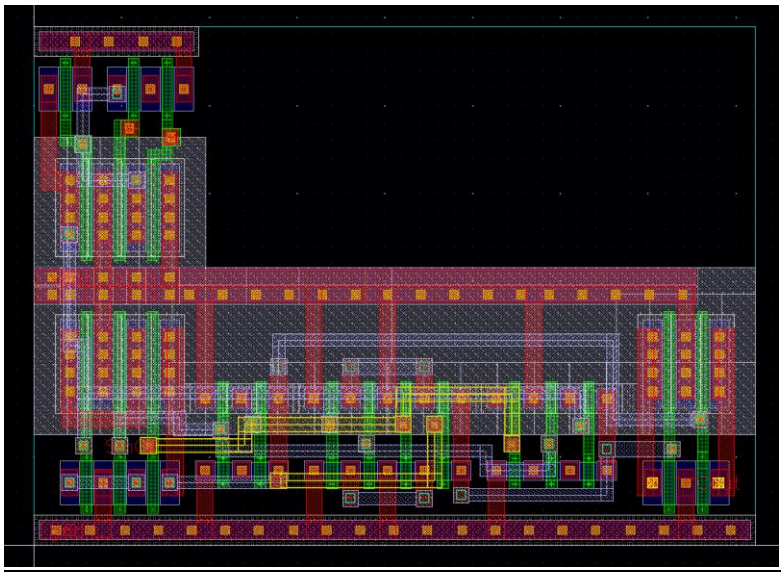


CSA

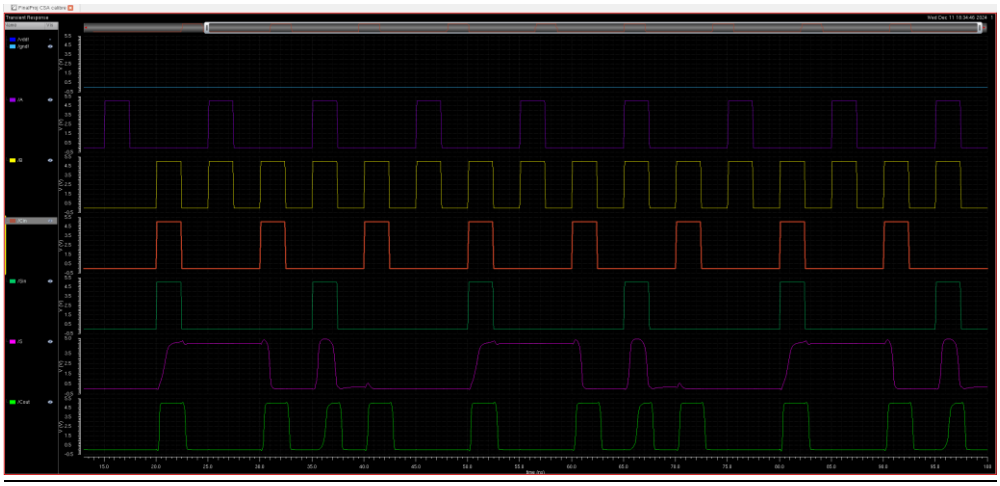
- Schematic



- Layout

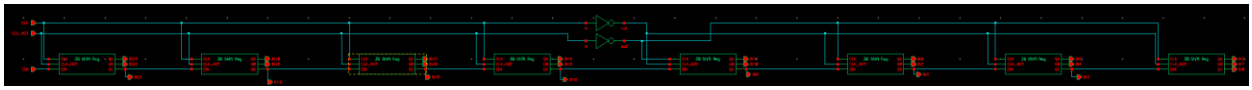


- Simulation

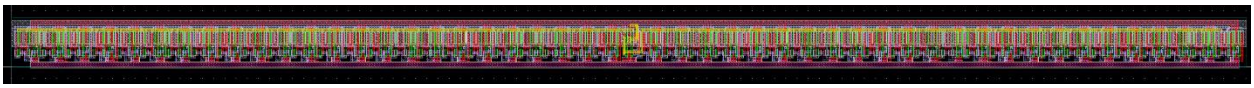


Input / Output Registers

- Schematic

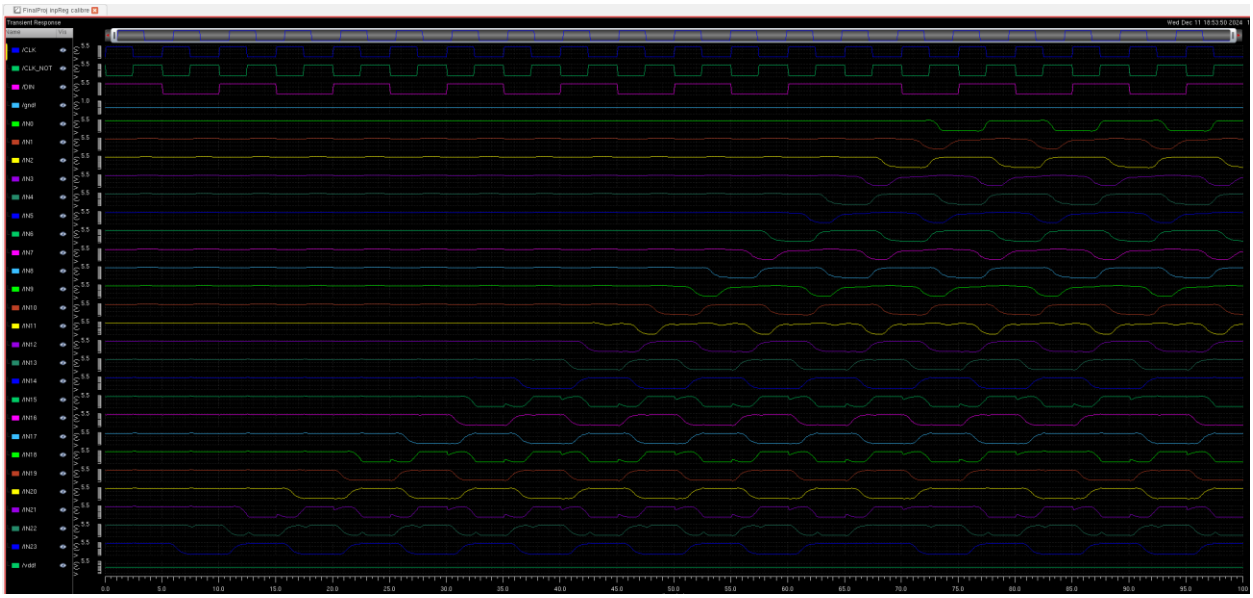


- Layout



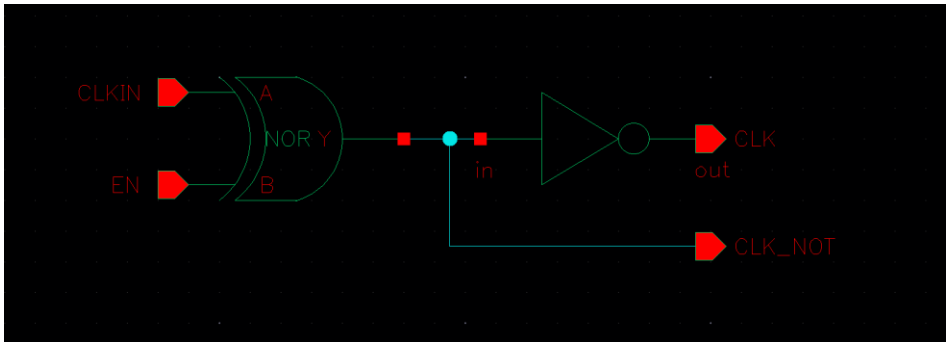
Zoomed in view visible in first section.

- Simulation

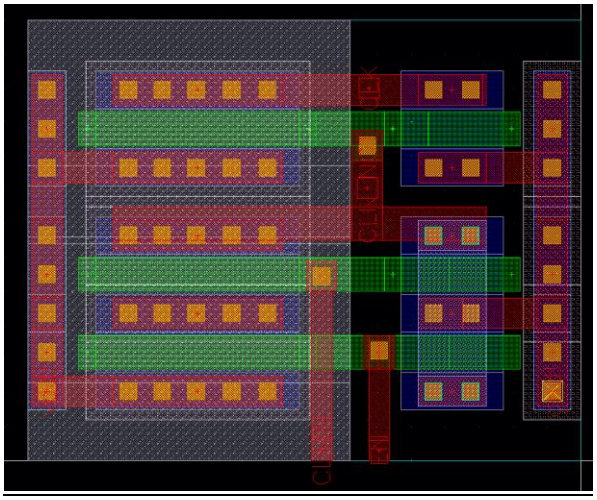


CLK Controller

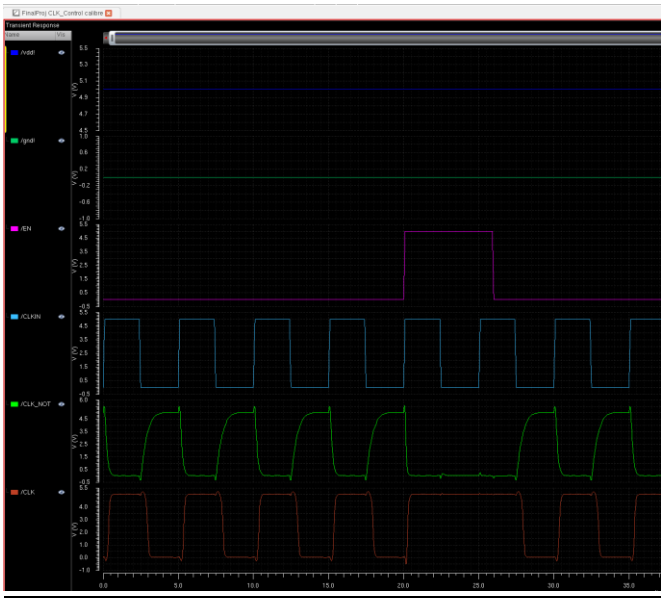
- Schematic



- Layout



- Simulation



Final Results

Below is the final schematic for the multiplier.

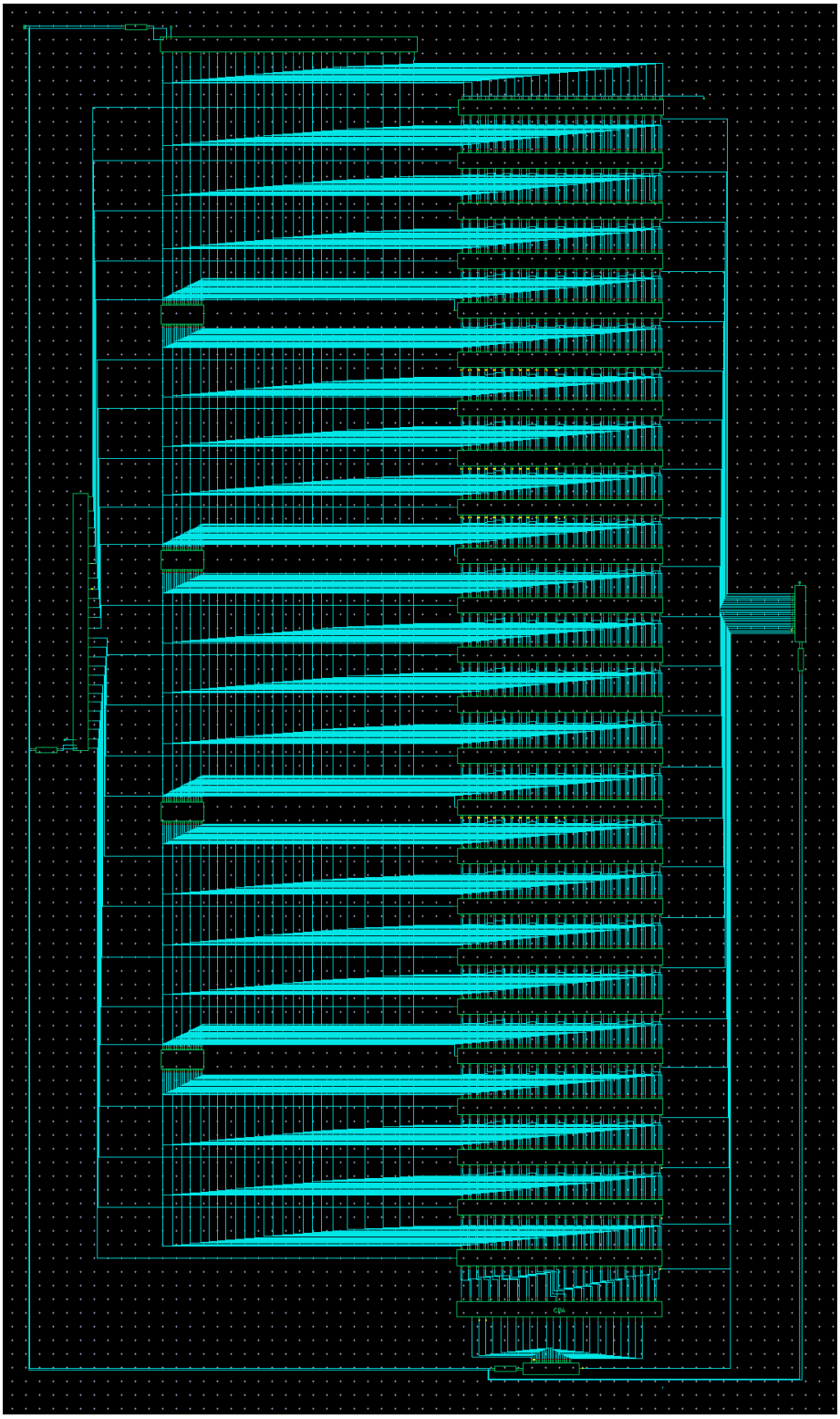


Figure 12: Final Multiplier Schematic

And, the final layout:

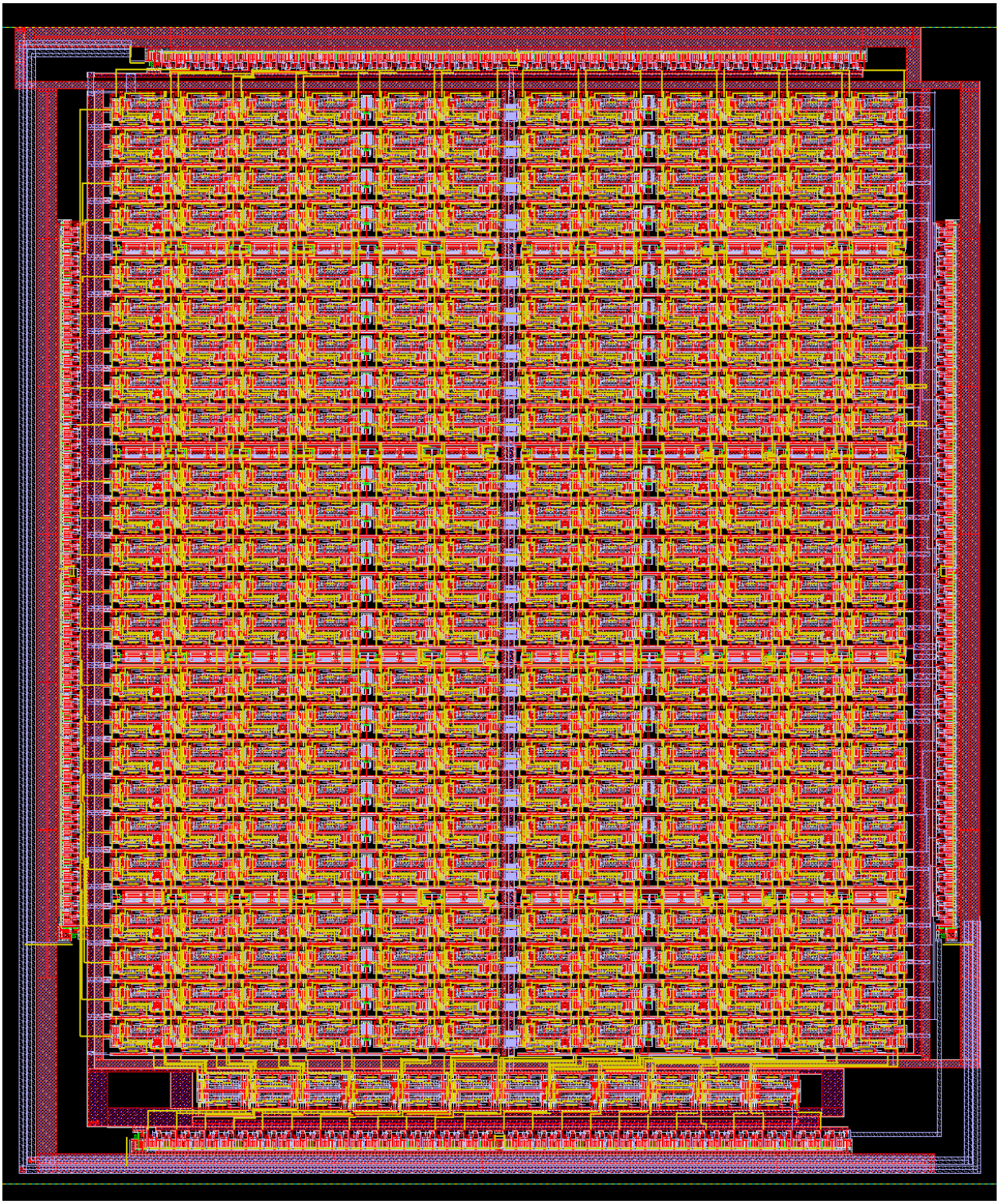
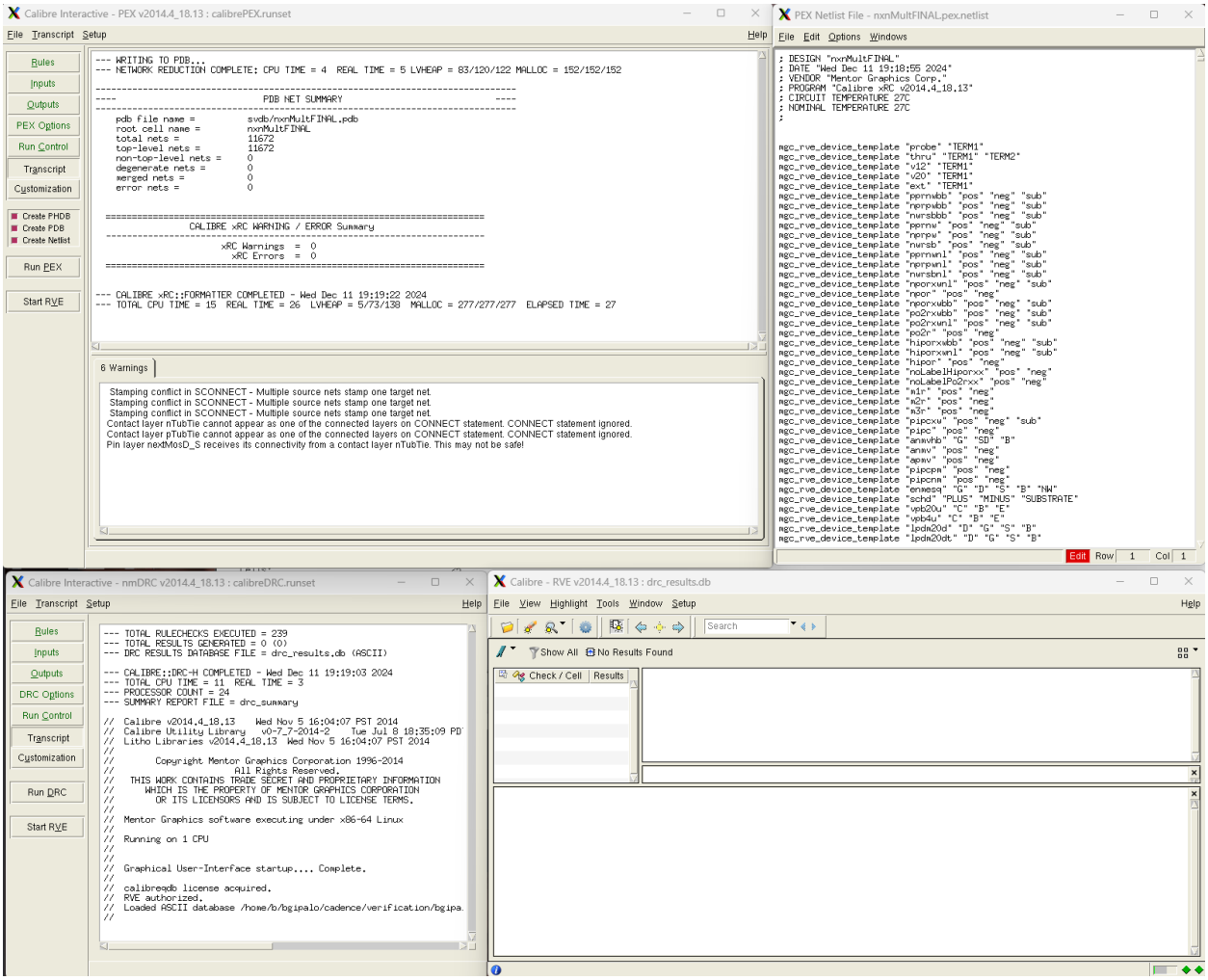


Figure 13: Final Multiplier Layout

With a total size (edge to edge) of 751.95 x 891.65.

The final layout passes nmDRC and PEX successfully, with 0 errors.



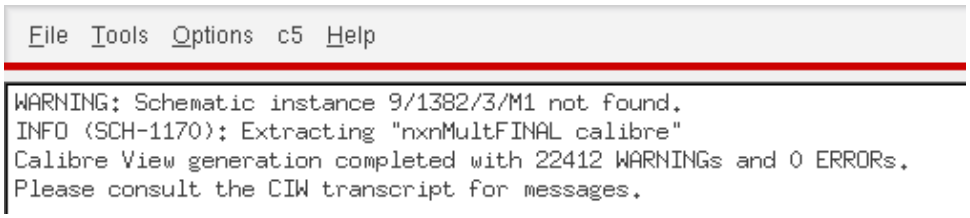


Figure 14: Successful DRC / Extraction